IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Tsutomu SASAO, et al.**

Serial Number: **Not Yet Assigned**
(§371 of International Application Number PCT/JP04/17263)

Filed: **May 18, 2006**

For. **A DEVICE FOR REDUCING THE WIDTH OF GRAPH AND A METHOD TO REDUCE THE WIDTH OF GRAPH, AND A DEVICE FOR LOGIC SYNTHESIS AND A METHOD FOR LOGIC SYNTHESIS**

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

May 18, 2006

Sir:

In compliance with 37 CFR 1.56, Applicants call to the attention of the Patent and Trademark Office the references listed on the attached PTO-1449 and cited in the enclosed international search report.

References AE-AT are discussed in the specification. References AH and AU are cited in the international search report. A copy of each of the references is enclosed herewith.

In the event there are any fees due in connection with the filing of this paper, please charge Deposit Account No. 01-2340.

Respectfully submitted,

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PATENT TRADEMARK OFFICE

Enclosures: PTO-1449 (3 sheets); References (17); International Search Report

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INFORMATION DISCLOSURE STATEMENT PTO-1449	Atty. Docket No. **060323**	Serial No. New Application 10/579743
	Applicant(s): **SASAO, Tsutomu, et al.**	
	Filing Date: **April 4, 2006**	Group Art Unit: **Not yet assigned**

OTHER DOCUMENTS

/PK/	AI	T. Sasao et al., "A Cascade Realization of Multiple-Output Function for Reconfigurable Hardware," International Workshop on Logic and Synthesis (IWLS01), Lake Tahoe, CA, June 12-15, 2001. pp.225-230 and three sheets of cover page and TOC.
/PK/	AJ	T. Sasao et al., "DECOMPOS: An Integrated System for Functional Decomposition", reprinted from1998 International Workshop on Logic Synthesis, Lake Tahoe, June 1998, pp. 1-7.
/PK/	AK	Y-T. Lai et al., "BDD Based Decomposition of Logic Functions with Application to FPGA Synthesis", 30th ACM/IEEE Design Automation Conference, June 1993, pp. 642-647.
/PK/	AL	T. Sasao, "FPGA DESIGN BY GENERALIZED FUNCTIONAL DECOMPOSITION", In Logic Synthesis and Optimization, Sasao ed., Kluwer Academic Publisher, 1993, pp.233-258 and eight sheets of cover page and TOC.
/PK/	AM	C. Scholl et al., "Communication Based FPGA Synthesis for Multi-Output Boolean Functions", reprinted from Asia and South Pacific Design Automation Conference, August 1995, 9 sheets (numbered as pp.279-287 in original).
/PK/	AN	B. Wurth et al., "Functional Multiple-Output Decomposition: Theory and Implicit Algorithm", Design Automation Conf., June 1995, 6 sheets (numbered as pp.54-59 in original).
/PK/	AO	H. Sawada et al., "Logic Synthesis for Look-Up table based FPGAs using Functional Decomposition and Support Minimization", reprinted from ICCAD, November 1995, 6 sheets (numbered as pp.353-358 in original).
/PK/	AP	J.-H.R.Jian et al., "Compatible Class Encoding in Hyper-Function Decomposition for FPGA Synthesis", Design Automation Conference, June 1998, 6 sheets (numbered as pp.712-717 in original).

Examiner	/Phallaka Kik/	Date Considered	03/27/2010

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /PK/

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OTHER DOCUMENTS

/PK/	AQ	P. Ashar et al., "Fast Functional Simulation Using Branching Programs", reprinted from Proc. International Conference on Computer Aided Design, November 1995, 5 sheets (numbered as pp.408-412 in original).
/PK/	AR	C. Scholl et al., "Functional Simulation using Binary Decision Diagram", reprinted from ICCAD'97, November 1997, 5 sheets (numbered as pp.8-12 in original).
/PK/	AS	A. Mishchenko et al., "Logic Synthesis of LUT Cascades with Limited Rails", IEICE Technical Report, VLD2002-99, Lake Biwa (2002-11), pp. 103-108 and two sheets of TOC.
/PK/	AT	M. R. Garey et al., "Computers and Intractability: A Guide to the Theory of NP-Completeness", W. H. Freeman & Co., New York, 1979, p. 194 and six sheets of cover page and TOC.
/PK/	AU	Y. Iguchi et al., "Realization of Multiple-Output Functions by Reconfigurable Cascades", reprinted from Proceedings of 2001 International Conference on Computer Design, 23 September, 2001 (23.09.01), Austin TX USA, pp. 388-393.

Examiner	/Phallaka Kik/	Date Considered	03/27/2010

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